ACTIVE VIBRATION CONTROL ACTUATION

Christopher D. Lesser and Darvin D. Remington
Moog Inc.
East Aurora, NY, USA

Abstract

Active vibration control systems require application of vibration reducing forces into the structure being controlled. These forces are provided by an AVCAS (Active Vibration Control Actuation System). The type of AVCAS selected depends upon a balancing of competing requirements such as performance, weight, envelope, cost and available power. The benefits and shortcomings of some practical AVCASs are reviewed. Controller and system designs are also discussed.

Dual point AVCAS provide 2 forces in equal and opposite directions between 2 points on an aircraft. Hydraulic actuation is presented as an example of a dual point AVCAS. Single point AVCAS use inertial forces to apply the vibration reducing force at a single location. Both electric and hydraulic linear versions are reviewed.

Also presented is a system that utilizes rotary inertial forces to generate a net linear inertial force. This is the most recently developed aircraft vibration reduction technique in production.

List of Acronyms & Symbols

Symbol	Description
ω	Frequency
a	Mass Acceleration
A	Peak Displacement
ADC	Analog to Digital Converter
ADS-37A-PRF	US Army Aviation and Troop Command – Aeronautical Design Standard – Performance and Verification Requirements
ASIC	Application Specific Integrated Circuit
AVC	Active Vibration Controller
AVCAS	Active Vibration Control Actuation System
AVCS	Active Vibration Control System
BIT	Built In Test
bps	Bits Per Second
C	Capacitive Filter
CAN	Controller Area Network
CBIT	Continuous Built In Test
CISC	Complex Instruction Set Computer
CPLD	Complex Programmable Logic Device
CRFG	Counter Rotation Force Generator
DAC	Digital to Analog Converter
dB	Decibels
DC	Direct Current
DEF-STAN-59-41	UK Ministry of Defense – Defense Standard – Electromagnetic Compatibility
DMA	Direct Memory Access
DSP	Digital Signal Processor
E^3	Electromagnetic Environmental Effects
EMP	Electro-Magnetic Pulse
ESD	Electro-Static Discharge
FDBK	Feedback
FG	Force Generator, Pair of CRFGs
FGC	Force Generator Controller
FIFO	First In – First Out
FPGA	Field Programmable Gate Array
Hz	Hertz (cycles per second)
I	Integral
I/O	Input / Output
IBIT	Initiated Built In Test
IEEE-1394	Institute of Electrical and Electronics Engineers – Standard for High Performance Serial Bus
IGBT	Insulated Gate Bipolar Transistor
Imun.	Immunity
K	Kilo (x1,000)
lbf	Pounds Force
LIFG	Linear Inertial Force Generator
M	Mega (x1,000,000)
M	Moving Mass
MIL-STD-461	US Department of Defense Interface Standard – Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment
MIPS	Million Instructions Per Second
MMACS	Million Multiply Accumulate per Second
NVRAM	Non Volatile Random Access Memory
P	Proportional
PBIT	Periodic Built In Test
PBIT	Power-up Built In Test
PI	Capacitive – Inductive – Capacitive Filter
PI	Proportional – Integral
PID	Proportional – Integral – Differential
PLD	Programmable Logic Device
PWM	Pulse Width Modulation
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RTCA/DO-160	Radio Technical Commission for Aeronautics – Environmental Conditions and Test Procedures for Airborne Equipment
RTCA/DO-178	Radio Technical Commission for Aeronautics – Software Considerations in Airborne Systems
SBIT	Start-up Built In Test
SRAM	Static Random Access Memory
t	Time
THD	Total Harmonic Distortion
TI	Texas Instruments
UART	Universal Asynchronous Receiver Transmitter
UK	United Kingdom
US	United States
USB	Universal Serial Bus
v	Mass Velocity
VDC	Volts Direct Current

Symbol	Description
XCVR	Transceiver
y	Mass Position

Introduction

Weight savings is the primary attraction for the application of AVCS (Active Vibration Control Systems) to aircraft. AVCS replace traditional passive absorbers and have reduced aircraft weight by as much as 150 pounds. Secondary benefits include improved vibration performance over a wider range of frequencies and longer component fatigue life. An AVCS reduces vibration by measuring vibration at key location(s) in the aircraft and applying cancellation forces within the aircraft. The system adjusts these forces as the aircraft maneuvers and as the aircraft payload varies. Aircraft payload changes as fuel is consumed and with different mission profiles.

Primary components of the AVCS, shown in the Figure 1, include Accelerometer(s), Active Vibration Controller (AVC) and AVCAS. The AVCAS can be thought of as providing the horsepower required for vibration reduction.

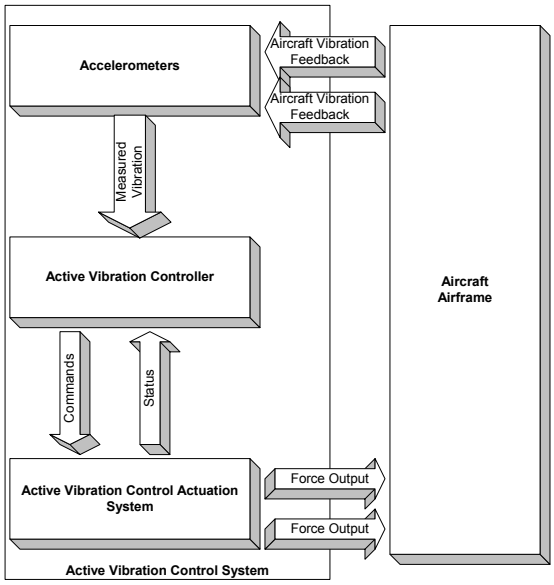

Figure 1: AVCS Component Block Diagram

This paper reviews types of actuation that have been used as an AVCAS. These include dual and single point actuators. Dual point actuators provide a force between 2 locations in the aircraft. Single point actuators apply a single force in the aircraft. The controller and system designs are also discussed.

Dual Point Actuators

As previously defined, dual point actuators exert a force between 2 points on the aircraft. One point is typically attached to the airframe and the second point is attached to the transmission. A hydraulic servo actuator is the most practical dual point AVCAS.

A hydraulic servo actuator used for vibration control is very similar to a fly by wire hydraulic flight control actuator. Figure 2 shows the major components of a hydraulic actuator used in an AVC. Major components consist of a hydraulic actuator, servo valve, power module and pressure transducers. Flight control actuators use position transducers instead of pressure transducers. The AVC drives current into the servo valve, which controls cylinder pressure to produce the required force. Pressure transducers feedback control port pressures to the AVC. With this feedback the AVC precisely controls actuator force output.

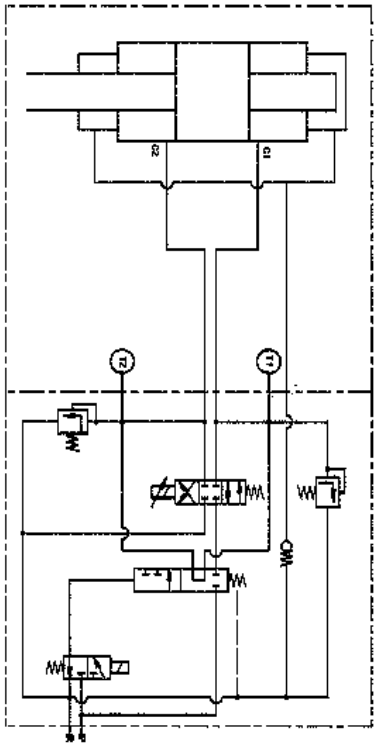

Figure 2: Hydraulic Servo Actuator

Service life of the actuator dictates the use of no dynamic elastomeric seals. Typical frequencies and nominal strokes are on the order of 17 Hz at ± 0.011". At this frequency the dynamic seal life expectation can be as high as 2 billion cycles. This type of life is several orders of magnitude greater than any elastomeric seal can achieve.

In addition to the unrealistic life expectations of an elastomeric seal, the worn seal material and debris can build up in the seal area (due to the short

stroke). This build up further erodes the seal and generates more build up. Dramatically short seal life occurs.

A lap fit between the piston and cylinder as well as the rod and rod gland solves the seal life issue. Typical lap fit clearances are on the order of 50 millionths of an inch. These clearances require special equipment and processing skills.

Hydraulic oil that leaks past the rod glands is contained within bellows that are sealed on the outside diameter of the rod gland and the rod. This oil is drained to the hydraulic oil return.

A primary challenge associated with lap fit seals is the issue of side loading. Side loading is caused by slight imperfections in geometry. Side loading causes metal to metal contact at the lap fit seal interfaces. Special materials and processes have been developed to prevent gauling.

Single Point Actuators

Single point actuators exert a force at a single location on the airframe. These actuators have an internal mass that is accelerated and decelerated in a controlled manner. The required forces to accelerated and decelerate the mass are reacted at a single point on the aircraft frame. Vibration reduction forces are the reaction forces due to inertial loads.

Two types of single point actuators are considered. The first is a linear device that moves the mass along a line. The second is a rotary actuator that produces a linear force. Generating a rotating force is not discussed in this paper.

LIFG (Linear Inertial Force Generators) LIFGs are composed of a spring mass system that is excited by an harmonic force. The spring mass system may have several masses and springs, resulting in more than one resonance. Only single resonant frequency devices are discussed here. A linear inertial force generator can produce large forces at tuned frequencies with little input power. The generator can be driven with a hydraulic or electric actuator.

Figure 3 schematically represents a linear inertial force generator. Notice that the LIFG is attached to the aircraft frame at one location. Primary components of this actuator are the moving mass, the spring and the actuator. These components can be designed to achieve the desired LIFG performance. Damping is also shown as a component. Damping is difficult to design and also to predict. The damping component is a combination of damping due to motion through the air and damping internal to the electric or hydraulic actuator.

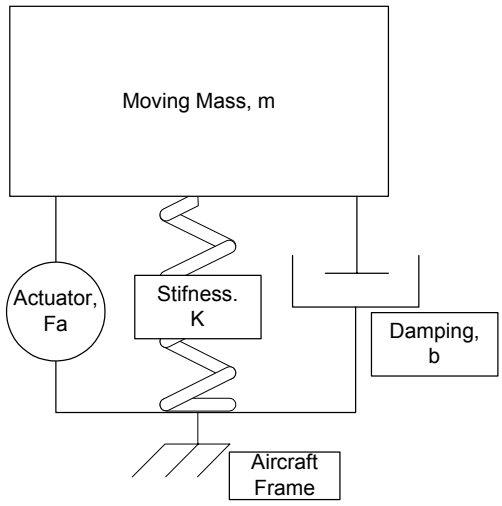

Figure 3: LIFG Schematic

This actuator has a single resonant frequency. The actuator provides the best performance near resonance. Resonance can be calculated by the equation $\sqrt{(K/M)}$. Figure 4 shows the force output into the aircraft frame per unit force output of the actuator. An amplification factor of 5 for this particular LIFG is indicated in Figure 4.

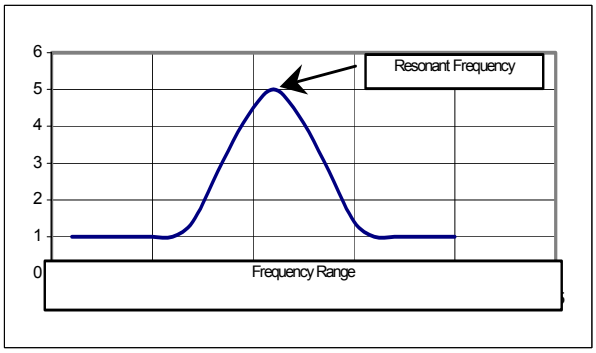

Figure 4: LIFG Amplification Factor vs Frequency

The tuning of the LIFG can be affected by the attachment point compliance. It is difficult to estimate the frequency shift. The frequency can shift either up or down. This is due to the attachment point having mass as well as stiffness. One solution is to design the actuator with a slightly higher resonance than required and add weights to tune the actuator frequency down. This allows customization by LIFG location in the aircraft.

It is important to understand the mass and stroke relationship for a particular force output. The

harmonic motion of the mass is described by the following equations.

$$y = A\sin(\omega t) \text{ [1]}; \quad v = A\omega\cos(\omega t) \text{ [2]}; \quad a = -A\omega^2\sin(\omega t) \text{ [3]};$$

The peak magnitude of the force, F_p, output can be calculated by multipling the moving mass by the peak acceleration. This result is listed as equation 4. Rearranging terms as shown in equation 5 shows that the mass product with peak displacement is a constant for a particular peak force at a frequency. Therefore the required moving mass can be decreased if the displacement is increased. And likewise the displacement can be decreased if the moving mass is increased.

$$F_p = mA\omega^2 \text{ [4]} \quad \Rightarrow \quad F_p/\omega^2 = mA \text{ [5]}$$

Electric LIFG A linear electric motor excites the resonance of the spring mass system in an electric LIFG. The electric motor is typically a voice coil design or a linear force motor design. The primary differences between a voice coil and a linear force motor are the moving components.

The coil within a voice coil moves with respect to the permanent magnet. Therefore, only the coil or the magnet can be part of the moving mass. This means that a significant part of the voice coil LIFG weight is destined to be part of the stationary mass. The stationary mass does not participate in the mechanical amplification. The relatively long stroke of the voice coil design can be used to partially offset the stationary mass disadvantage.

A linear force motor design uses 2 magnets and a coil. All of the magnets and coil can be part of the moving mass. The result is that about 90 % of the entire actuator weight can be a part of the mechanical amplification. The linear force motor stroke is limited in comparison to the voice coil design. This means that the motion of the moving mass is reduced, and the moving mass is less effective.

Harmonic distortion is caused by nonlinearities within the actuator. Magnetic nonlinearities can dominate. Other nonlinearities include spring hysteresis and friction. By properly designing the stroke and air gaps of the actuator, the magnetic effects can be approximately linear. Combined with minimizing friction and low hysterisis springs, the THD (Total Harmonic Distortion) is typically better than -25 dB.

A feedback transducer is not typically a part of an electric LIFG. Feedback is not required for operation and adds cost and weight. The AVC measures the LIFG's performance indirectly through accelerometer feedback. The lack of direct feedback does require drive limiting on the AVC to prevent over stroking the electric LIFG. Over stroking the actuator reduces life and increases harmonics.

Both designs have a mechanical null position. This position is determined by the mechanical spring rate, the magnetic spring rate and the gravitational force applied to the moving mass. When electric power is removed the actuator returns to this position.

With only slight differences in the magnetic circuit, the voice coil LIFG and linear force motor LIFG offer comparable performance. The longer stroke of the voice coil design is offset by a heavier stationary mass than the linear force motor. The shorter stroke of the linear force motor is offset by a lighter stationary mass.

Hydraulic LIFGs A hydraulic actuator excites the resonance of the spring mass system in a hydraulic LIFG. A hydraulic actuator can provide significantly higher driving forces than an electric motor. Therefore, the moving mass of this LIFG can be orders of magnitude larger than the electric LIFG's previously discussed. This results in significantly higher output forces. THD is similar to an electric LIFG.

Hydraulic LIFG's use a position transducer to feedback actuator position to the control electronics. This position information can be used to precisely control the moving mass stroke. Precise control of moving mass stroke guarantees the force output of the LIFG. This also allows the control electronics to maintain the hydraulic cylinder near null. This may be required because open loop hydraulics tend to drift and the actuator could run up against a stop.

The previous seal life discussion on the dual point hydraulic servo actuator applies to this device. This issue is solved with lap fit seals (see dual point actuators for explanation).

CRFG (Counter Rotating Force Generator) A CRFG spins two eccentric masses about a common axis in opposite directions at the same velocity. CRFG mass position is controlled to produce only a linear force. This will be described in the remaining text.

CRFG's require electronics to interpret the commanded force(s) from the AVC and control the mass velocities and positions. The required electronics is called a FGC (Force Generator Controller). Figure 5 shows a block diagram of the AVCAS and its associated CRFG and FGC components.

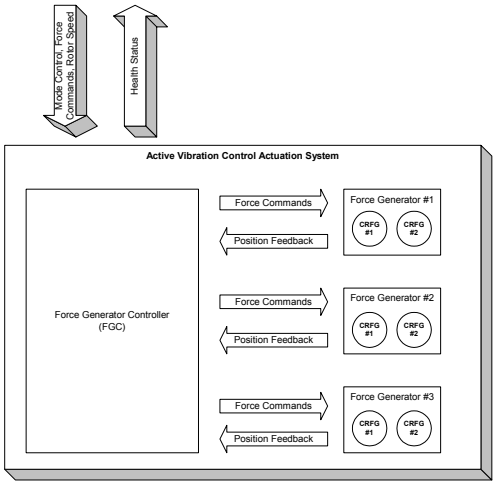

Figure 5: AVCAS Block Diagram

Typically, brushless electric motors are used to spin the eccentric masses. This requires additional electronics and software, which are not usually provided in the AVC. A separate FGC assembly is used because the AVC is a general design not specific to the type of actuator technology. Concerns with the power dissipation of the FGC electronics further supports the desire to separate the AVC and FGC. This does not preclude the combination of the AVC and FGC into a single enclosure. Additional size, weight and cost reduction demands have initiated design studies to integrate the AVC and FGC into a single enclosure.

Force output of a linear CRFG can be derived using some basic kinematics and dynamics. Note first that there are a total of 3 co-ordinate systems required to describe the motion of the masses within the CRFG, see Figure 6. The first co-ordinate system axes are x, y and z. The z axis is defined as positive coming out of the paper. A unit vector is assigned to each axis, $\underline{i}$, $\underline{j}$ and $\underline{k}$ respectively. A co-ordinate system is assigned to each mass and rotates with the mass. Mass #1 has the r_1, θ_1 and z_1 axes associated with it along with the unit vectors $\underline{i}_{r1}$, $\underline{i}_{\theta 1}$ and $\underline{i}_{z1}$. Mass #2 has the r_2, θ_2 and z_2 axes associated with it along with the unit vectors $\underline{i}_{r2}$, $\underline{i}_{\theta 2}$ and $\underline{i}_{z2}$. The z_1 and z_2 axis are coincident with the previously defined z axis. The origin of all three co-ordinate systems is at point o.

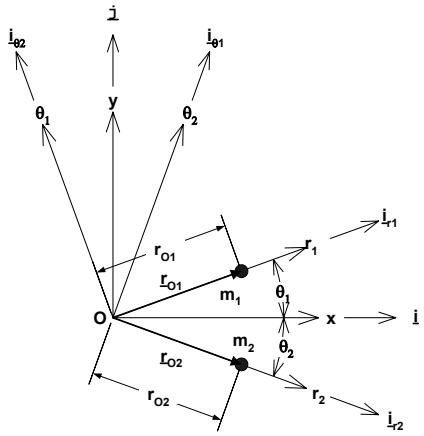

Figure 6 : CRFG Vector Diagram

The following kinematics equations describe the motion of the masses. These equations are based on constant $\underline{r}_{o1}$ and $\underline{r}_{o2}$. Displacement vectors $\underline{r}_{o1}$ and $\underline{r}_{o2}$ are differentiated to obtain velocity vectors that are differentiated to obtain acceleration vectors.

$\underline{r}_{o1} = \{r_{o1}\underline{i}_{r1}\}$ *[6]* $\underline{r}_{o2} = \{r_{o2}\underline{i}_{r2}\}$ *[7]*

$\underline{v}_1 = \{\omega_1 r_{o1}\underline{i}_{\theta 1}\}$ *[8]* $\underline{v}_2 = \{\omega_2 r_{o2}\underline{i}_{\theta 2}\}$ *[9]*

$\underline{a}_1 = \{\alpha_1 r_{o1}\underline{i}_{\theta 1} - \omega_1^2 r_{o1}\underline{i}_{r1}\}$ *[10]*

$\underline{a}_2 = \{\alpha_2 r_{o2}\underline{i}_{\theta 2} - \omega_2^2 r_{o2}\underline{i}_{r2}\}$ *[11]*

Force applied to each mass to produce the desired motion is given by equations 12 and 13.

Figure 7 defines the forces acting on the rotating masses. These forces are reacted at point o and the vector sum of these forces is the force applied to the structure by the CRFG.

$\Sigma\underline{F}_{m1} = \{m_1\underline{a}_1\}$ *[12]* $\Sigma\underline{F}_{m2} = \{m_2\underline{a}_2\}$ *[13]*

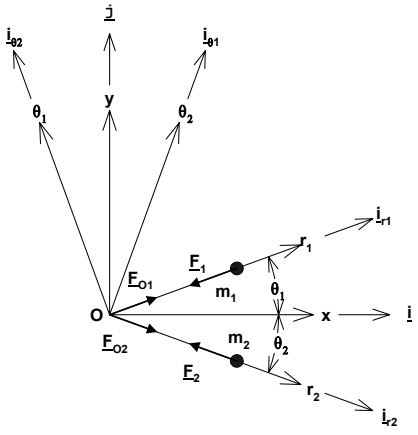

Figure 7: CRFG Free Body Diagram

The only forces acting on mass 1 and mass 2 are $\underline{F}_1$ and $\underline{F}_2$ respectively. Substituting these forces into the left-hand side of the equations and the previously derived mass accelerations into the right side of the equation yield equations 14 and 15.

$$\underline{F}_1 = \{m_1(\alpha_1 r_{o1}\underline{i}_{\theta 1} - \omega_1^2 r_{o1}\underline{i}_{r1})\} \quad [14]$$

$$\underline{F}_2 = \{m_2(\alpha_2 r_{o2}\underline{i}_{\theta 2} - \omega_2^2 r_{o2}\underline{i}_{r2})\} \quad [15]$$

These forces are reacted by equal and opposite forces $\underline{F}_{o1}$ and $\underline{F}_{o2}$ described by equations 16 and 17 below.

$$\underline{F}_{o1} = -\underline{F}_1 \quad [16] \qquad \underline{F}_{o2} = -\underline{F}_2 \quad [17]$$

The total force applied to the structure by the CRFG is the sum of $\underline{F}_{o1}$ and $\underline{F}_{o2}$.

$$\underline{F}_C = \underline{F}_{o1} + \underline{F}_{o2} = -\underline{F}_1 - \underline{F}_2 \quad [18]$$

$$\underline{F}_C = \{-m_1(\alpha_1 r_{o1}\underline{i}_{\theta 1} - \omega_1^2 r_{o1}\underline{i}_{r1}) - m_2(\alpha_2 r_{o2}\underline{i}_{\theta 2} - \omega_2^2 r_{o2}\underline{i}_{r2})\} \quad [19]$$

$$\underline{F}_C = \{m_1(\omega_1^2 r_{o1}\underline{i}_{r1} - \alpha_1 r_{o1}\underline{i}_{\theta 1}) + m_2(\omega_2^2 r_{o2}\underline{i}_{r2} - \alpha_2 r_{o2}\underline{i}_{\theta 2})\} \quad [20]$$

Given the following:

$$m = m_1 = m_2 \quad [21] \qquad r = r_{o1} = r_{o2} \quad [22]$$

$$\theta = \theta_1 = \theta_2 \quad [23] \qquad \omega = \omega_1 = -\omega_2 \quad [24]$$

$$\alpha = \alpha_1 = -\alpha_2 \quad [25]$$

$$\underline{i}_{r1} = \cos(\theta_1)\underline{i} + \sin(\theta_1)\underline{j} \quad [26]$$

$$\underline{i}_{r2} = \cos(\theta_2)\underline{i} - \sin(\theta_2)\underline{j} \quad [27]$$

$$\underline{i}_{\theta 1} = \cos(\theta_1)\underline{j} - \sin(\theta_1)\underline{l} \quad [28]$$

$$\underline{i}_{\theta 2} = \cos(\theta_2)\underline{j} + \sin(\theta_2)\underline{l} \quad [29]$$

$$\underline{F}_C = \{m(\omega^2 r(\cos(\theta)\underline{i} + \sin(\theta)\underline{j}) - \alpha r(\cos(\theta)\underline{j} - \sin(\theta)\underline{i})) + m(\omega^2 r(\cos(\theta)\underline{i} - \sin(\theta)\underline{j}) + \alpha r(\cos(\theta)\underline{j} + \sin(\theta)\underline{i}))\} \quad [30]$$

$$\underline{F}_C = \{2m(\omega^2 r\cos(\theta) + \alpha r\sin(\theta))\underline{i}\} \quad [31]$$

Equation 31 was derived to support harmonic distortion discussions later in this text. For the immediate discussion of force output it is assumed that θ is constant and therefore α is zero. With constant angular velocity the position θ can be expressed as $\omega t+\phi$. The phase angle ϕ is introduced here to account for the possibility of nonzero force output at time equal 0. Given this, the CRFG force output as a function of time can be expressed as:

$$\underline{F}_C = \{2m\omega^2 r\cos(\omega t + \phi)\underline{i}\} \#'s \quad [32]$$

The peak magnitude of this force, $2m\omega^2 r$, is fixed for a particular output frequency. Figure 8 plots force vs time.

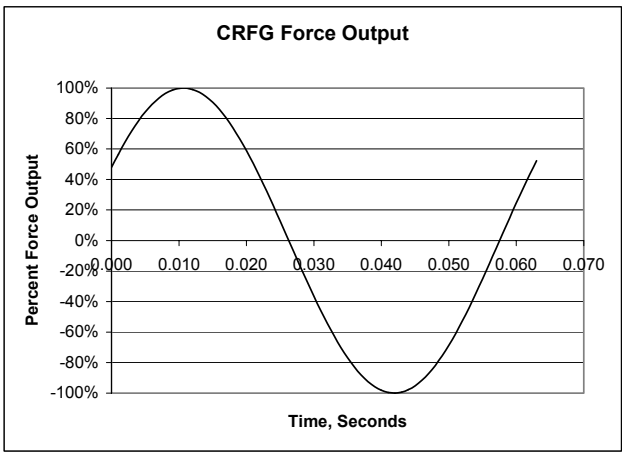

Figure 8: Single CRFG Force Output

A pair of CRFG's, also known as an FG (Force Generator), is required to produce a scalable force output at a particular frequency. The force output of each CRFG can be written by adding and subtracting a phase angle to the equation describing the CRFG's output force.

$$\underline{F}_{C1} = \{2m\omega^2 r\cos(\omega t + \phi)\underline{i}\} \quad [33]$$

$$\underline{F}_{C2} = \{2m\omega^2 r\cos(\omega t - \phi)\underline{i}\} \quad [34]$$

$$\underline{F}_T = \underline{F}_{C1} + \underline{F}_{C2} \quad [35]$$

$$\underline{F}_T = \{(2m\omega^2 r\cos(\omega t + \phi) + 2m\omega^2 r\cos(\omega t - \phi))\underline{i}\} \quad [36]$$

$$\underline{F}_T = \{(4m\omega^2 r(\cos(\omega t + \phi) + \cos(\omega t - \phi))\underline{i}\} \quad [37]$$

$$\underline{F}_T = \{4m\omega^2 r\cos(\phi)\cos(\omega t)\underline{i}\} \quad [38]$$

Total force output, $\underline{F}_T$, of an FG is given in equation 38 and is plotted in Figure 9. The maximum peak force output capability of an FG is $4m\omega^2 r$. The moving mass, m, and radius, r, are fixed by the design of the CRFGs. It can be seen from this equation that the peak capability of a given FG is proportional to the operating frequency. The peak operating output force is given by $4m\omega^2 r\cos(\phi)$ and is controllable by adjusting the value ϕ between 0 and $\pi/2$. It is convenient to define a ratio R. R represents a fraction of the maximum output force capability of an FG at frequency ω and ranges from 0 to 1. The ϕ value can be determined by the following values.

$$R = |\underline{F}_T|/4m\omega^2 r \quad [39] \qquad \phi = \cos^{-1}(R) \quad [40]$$

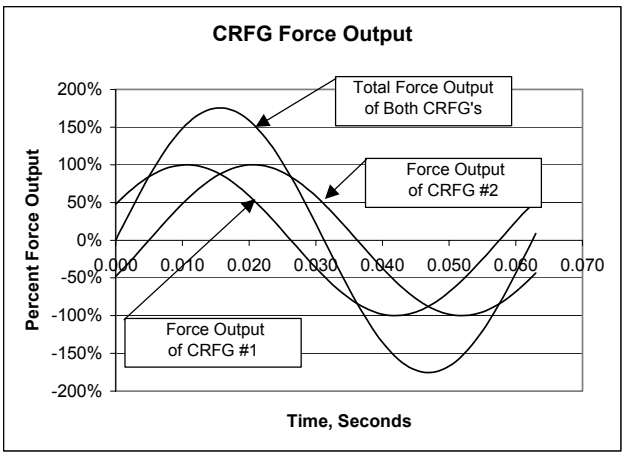

Figure 9: Combined CRFG Force Outputs

The source of harmonic distortion in a CRFG is dominated by variation in angular velocity. It was previously derived that the force output of a CRFG with variable angular velocity is given by equation 31.

Let us assume the angular velocity variation of a CRFG is due to gravity and a loose velocity and position loop in the control system. The angular velocity and acceleration can be written as a function of position per the following:

$\omega = \omega_C - \Delta\omega\sin(\theta)$ *[41]* $\alpha = \Delta\omega\cos(\theta)$ *[42]*

Equations 31, 41 and 42 have been used to estimate THD. Analysis has shown that the angular velocity can vary by $\pm$2.5% and maintain better than –25 dB THD.

FGC Design Considerations

The design of the FGC needs to primarily address the following areas: system architecture, software architecture, controller communications interface, E^3 (Electromagnetic Environmental Effects) and controller size and weight. Each of these areas can influence the other and compromises must be made to optimize the controller for the specific system requirements. This paper discusses typical values and/or solutions for each of the above areas.

System Controller Architecture When beginning any controller design a system and controller architecture must be determined. The designer must determine what functions of the system are implemented in software or hardware, determine how the processing of the functions should be distributed throughout the controller, choose the appropriate processor, memory and peripherals. To answer these questions, the designer must take into account the number of drive channels, communications requirements, control-loop structures and update rates, BIT (Built-In-Test) requirements, growth requirements, part obsolescence, reliability requirements, maintenance requirements, cost, etc.

As an example, a system may only require one or two motor drive channels, a simple serial command interface, small BIT and limited growth requirements, with extremely low production cost goals. A designer may consider an architecture that utilizes a single DSP with embedded memory, serial I/O and motor control peripherals. TI is the leading supplier of this type of low cost DSPs (Digital Signal Processors). Additional components for the system would only require the I/O buffering for the serial communications, the power supply components, feedback conditioning and power driver components. Figure 10 shows a block diagram of this system.

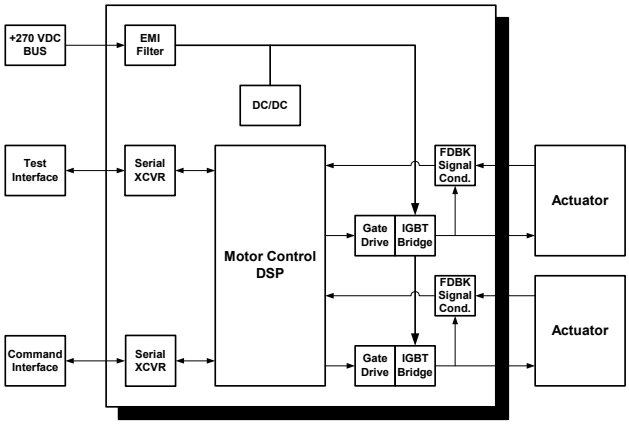

Figure 10: Simple FGC Block Diagram

As a second example, a system may require from one to six dual motor drive channels, a more complex high-speed interface, full BIT, a 50% growth requirement and moderate production cost sensitivity. A designer may consider a more distributed architecture. In this case each of the dual motor channels utilizes a motor control DSP or custom FPGA/ASIC in conjunction with feedback conditioning and power driver components. Each of these dual motor channels interfaces with a common processor or DSP that handles the command communications, BIT, process scheduling and higher-level control-loop functions. If the majority of the time critical motor and control-loop functions are performed at the dual motor drive level, adding or subtracting channels has only a small loading effect at the common processor level. This allows for a more flexible design that can be scaled to meet different system design requirements while taking advantage of basic design commonality to reduce cost. Figure 11 shows a block diagram of this system.

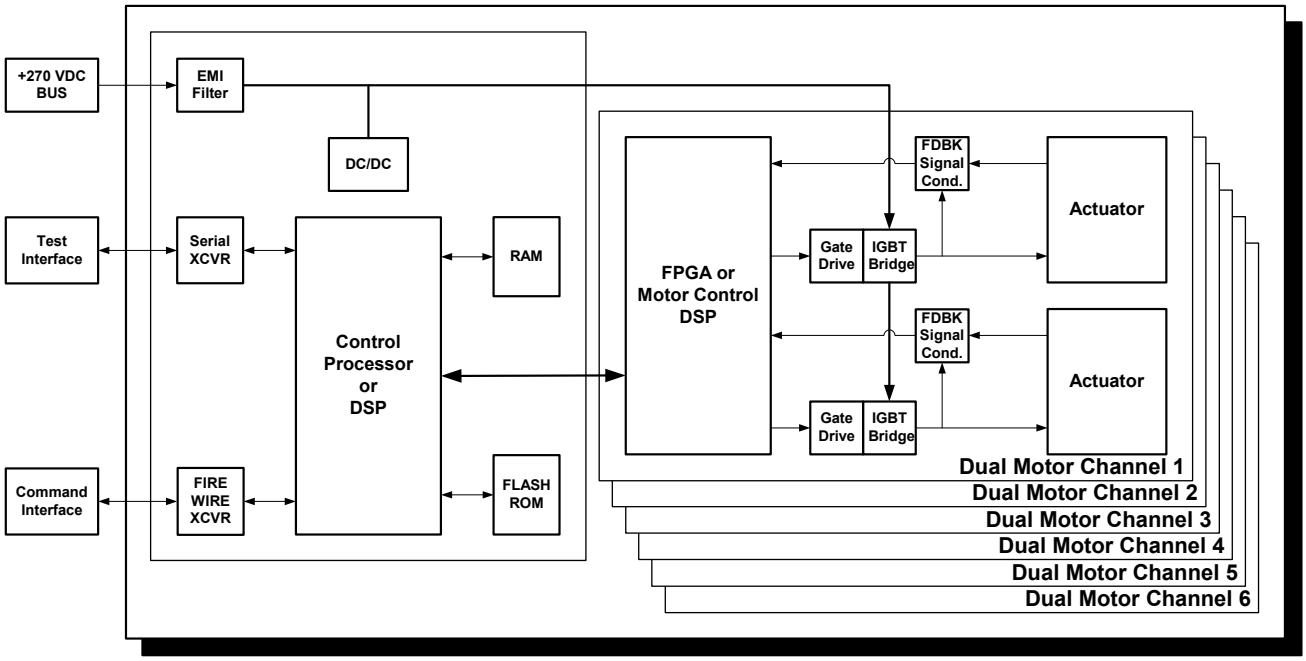

Figure 11: Multi-Channel FGC Block Diagram

Processor Selection A major portion of the overall control architecture usually centers on the main control processor and any secondary processors used to directly control the motor. The proper selection of these processors is key to making an architecture work for the design at hand. Several basic categories of processors are available and should be selected to best fit their intended functions. They include Digital Signal Processors (DSP), Complex Instruction Set Computer (CISC) and Reduced Instruction Set Computer (RISC) processors. For the portions of an architecture where math intensive operations are being performed, such as control-loop calculations and motor commutation calculations, a DSP is best suited. For operations where simple data moving and discrete bit checking are being performed, such as communications interfaces, task scheduling and some BIT functions, a CISC or RISC may best suited.

In addition to processor type, the designer must also look at processor specifics that will be required to meet the overall system requirements. In the case of a DSP, a designer is required to examine whether the part performs either fixed-point or floating-point math. This will influence the level of software effort required and attainable accuracy. Fixed-point math requires the software designers to take into account scaling issues and limits where as floating-point values are virtually unlimited. The data bit width of the processor and its internal components need to be considered, as this characteristic will determine the resolution of control calculations being performed by the system. Processors generally have data widths of 8, 16, 32 or 64 bits. Internal peripheral components will also have data widths between these values such as 10, 12, 14 bits ADCs and DACs along with 24 bit counter/timers. Insufficient resolution could limit performance and in some cases make control marginal.

Embedded processor memory and peripherals need to be considered when choosing a processor. This is especially true in the first system architecture example where a single DSP is used and low cost is required. The designer should consider what kind of embedded memory is available, such as SRAM (Static Random Access Memory), ROM (Read Only Memory), FLASH, NVRAM (Non-Volatile RAM), and what is its size verses what is required. Is there enough memory to do the job the controller was intended for? Processors have embedded SRAM blocks ranging from ½K words up to 264K words. Embedded ROM and FLASH blocks range from 4K words up to 128K words.

The designer must ask what kinds of embedded peripherals are available. Peripherals such as serial ports, USB (Universal Serial Bus) controllers, CAN (Controller Area Network) bus controllers, DMA (Direct Memory Access) controllers, counter-timers, ADCs (Analog to Digital Converters) and DACs (Digital to Analog Converters) are all important components. If required by the design, these components would have to be provided by additional devices when not available within the DSP. Very important sets of peripherals are those targeted at motor control. The motor control peripherals include functions such as digital data capture units for event and

feedback data, event timers and PWM (Pulse Width Modulation) generators. Several manufactures provide motor control DSP lines that include these embedded motor control peripherals. They include Texas Instruments, Analog Devices, National Semiconductor, ST Microelectronics and Microchip.

Lastly, the designer must consider the processor's speed performance. A processor's speed performance will influence how many functions can be performed by the system design and how fast the functions can be updated. This is particularly important when control algorithms are considered. The processor needs to be fast enough to allow for all the control algorithms to complete at a rate where control is stable and of adequate accuracy and resolution. A processor is rated by how many instructions it can perform within a second at some specified clock frequency. The common unit of measure used is MIPS or Million Instructions Per Second. TI offers processors with performance that approximately ranges from 40 MIPS, 40,000,000 instructions executed in one second, to 400 MIPS. A second performance rating considers the math operations speed. For Fixed-Point processors this is the MMACS or Million Multiply Accumulate Cycles per Seconds. Typical values of 320 MMACS are common for Fixed-Point processors. A Floating-Point processor uses a MFLOPS or Million Floating-Point Operations per Second as a rating. A typical TI Floating-Point processor performs at 825 MLOPS.

External Memory and Peripherals All of the above embedded processor features need to be weighed against the overall system requirements. If the embedded processor features do not meet the system requirements, then in many cases, external memory and peripheral components are required. Here again the designer must choose these components carefully and assure the choices will meet the system requirements. Memory must be chosen to be the proper type, size, data width and speed to interface with the processor and not hinder the processor as to make the system too slow to perform its intended function. ADCs and DACs must have the necessary resolution and speed to meet the system control requirements. UARTs (Universal Asynchronous Receiver Transmitters) need to satisfy the system communication requirements such as data transmission rate, data bit width, data protocol, receiver and transmitter FIFO (First In, First Out) buffer depth. Other communications peripherals may include Firewire controllers, USB controllers, CAN bus controllers each with their own unique set of interface requirements. Lastly, when custom, flexible design or high-density functional blocks are required, devices such as PLDs (Programmable Logic Devices), CPLDs (Complex Programmable Logic Devices), FPGAs (Field Programmable Gate Arrays) and ASICs (Application Specific Integrated Circuit) can be used by the designer.

Software Considerations Hand in hand with the processor and support peripheral hardware is the software component of the system architecture. In designing a controller, several software design decisions must be considered as they may affect what hardware is required as well as the level at which the system can perform. The system designer should include the following software items when design choices are being made:

- Software architectures
- Software language selections
- Software tools
- Software standards

Each of these items must be considered individually as well as how they effect one another.

When considering the software architecture, the designer must examine how the software is organized. Should the code be constructed using deterministic "Straight Coding" with function, procedure and subroutine calls for recurring blocks of code? Or should the software utilize "Task Scheduling" driven by a timer driven interrupt calling the appropriate functions, procedures and subroutines at scheduled time-sliced intervals? Should state machine logic be utilized or multiple level decision blocks be used? Should data structures be organized by functional or data types? Should global variables be used, or should parameters be passed to and from routines, or should pointers be used? Should a routine be a function, a procedure, a subroutine, a generic or should it be "in-line-coded" for speed? All these questions need to be considered.

As part of the software considerations, the software language selections are very important. The software language chosen by the designer can both affect and is effected by the processor, software architecture and software tools utilized. Generally for processors both assembly level and higher-level software languages can be used. Common higher-level software languages utilized in embedded controller designs include C/C++, ADA and PASCAL, the most common of which is C/C++. Assembly language alone is generally not utilized unless the software is very time critical and needs to be highly optimized. This may also be the case if the higher-level language compiler is not very efficient in how it generates its assembly code. The software language chosen is generally limited by what either the processor manufacture has available or by what industry third party vendors can provide in support tools.

The software tools considered usually include tools for software coding, compiling software, testing software code, documenting the software design and code and tools for software configuration management. Some of these tools are specific to the processor or language type chosen for the design. Others may be generic in nature and may be used across designs and processor platforms. Software standards for coding, testing, documenting and configuration management of a design are important in controlling the software design process in order to produce consistently reliable software. In addition, the standards can help reduce costs through code reuse and lower code maintenance costs. Following commercial or military software standards such as DO-178 are utilized to insure the integrity of the software and verify that the system requirements are met. Levels within these standards are set applying different documentation and testing rigor as necessary for a specific design requires. For DO-178 there are 5 levels that run from Level-A, that is flight critical, to Level-E, that is general software.

Control Algorithms The purpose of the controller is to control the actuator with a certain measure of stability and accuracy. The control algorithms chosen are influenced by the stability and accuracy required as well as the feedback devices, processor speed and support hardware bandwidths. In general, the types of control algorithms required include:

- Position or phase control loops
- Velocity control loops
- Current or torque loops
- Motor commutation control algorithms

The control loops may include P (Proportional), I (Integral), PI (Proportional-Integral), PID (Proportional-Integral-Differential) or simple output limited elements. The motor commutation algorithms may utilize basic 6-step commutation or full sine-drive commutation.

As an example, a typical application might require an outer PI compensated position control loop feeding into a PI compensated velocity control loop that drives a current control loop that commands a sine- drive motor commutation control algorithm. A different application may require a P phase control loop, with a PI compensated velocity control loop that drives an output limited current control loop that commands a 6-step motor commutation control algorithm. In general, the more complicated and higher accuracy requirements of the control algorithms, the more expensive in both cost and processing power the system will be.

BIT (Built-In-Test) Considerations BIT or Built-In-Test are functions in either hardware or software that verify the health and proper operation of the controller and actuator system. There are three categories of BIT. They include Start-Up BIT (SBIT) or Power-Up BIT (PBIT), Initiated BIT (IBIT), and Periodic BIT (PBIT) or Continuous BIT (CBIT). Determination as to whether a BIT function or monitor is to be performed in hardware or software is usually evaluated on implementation practicality and reliability requirements. Many times if a system fault is categorized as a hazardous/severe failure, one or more hardware monitors would be required to meet the reliability and safety requirements. If a hardware method is not achievable then a software monitor may drive the software standard level up from a Level-D or C up to a Level-B or A.

SBIT is as its name implies, is run during start-up or power-up after the processor(s) have booted and prior to normal run modes. SBIT tests initial hardware integrity looking for faults. Tests may include RAM, ROM or FLASH memory tests, power supply monitor tests, watch-dog timer tests, communications loop-back tests, and other design specific tests. Failure of any of these tests may limit system or controller operation or may completely disable the system.

IBIT is used to more functionally verify the system as a whole, usually on the ground. As its name implies, IBIT is initiated by some outside control, either a higher level controller or operator input. Tests may include running the system and measuring command-response rates, feedback signal integrity, etc. Failure of the IBIT tests can disable the entire system, result in some system reconfiguration or provide a degraded system operation.

PBIT or CBIT are run as part of the normal system operation modes. System, component and algorithm health are verified as the controller operates. PBIT tests can include communications integrity, power supply voltage levels, controller or actuator temperatures, motor currents, feedback sensor faults, control algorithm tolerances, etc. Rates of these BIT functions or monitors, their persistence and fault trip levels are determined by the designer. The designer must optimize these rates and levels to catch a fault before serious damage might occur but not produce nuisance faults.

AVC to FGC Communications Interface The controller by itself is useless unless it can be commanded to perform its function from an AVC. The interface between the CRFG FGC and the AVC is a two-way interface that provides command and control information to the FGC and in turn provides status information back to the AVC. This

information may be transferred by several different methods. Older style controllers may have analog command and feedback signals coupled with discrete digital status and control lines. These types of interfaces are limited in the amount of complex information that can be transferred by modern processors and are much more susceptible to noise and drift problems. Modern controllers rely on many digital interfaces. These interfaces are generally high-speed serial data streams that provide verifiable data that is relativity immune to noise or drift problems. Data is usually sent in data packet form containing a Start-of-Message marker, data word count, data words, checksum word and an End-of-Message marker.

Typical command data sent from the vibration controller to the FGC would include:

- Message identification data
- Discrete enable and configuration data
- Position or phase command data
- Velocity command data
- Force output command data.

Depending on the number of channels being commanded, the resolution of the data and whether the data was being multiplexed between channels, the data word length could be from 10 to 100 data words. This information would be sent at a rate allowing the overall vibration cancellation loops to be closed in a stable manor.

Typical status data sent from the motor controller to the vibration controller would include:

- Motor enable and configuration echo back
- Fault status
- Command echo back
- FGC or CRFG temperature data
- Feedback data

Type	Multi-Ports	Noise Imun.	Data Rate	Complexity		Cost
			bps	HW	SW	
RS-232	N	L	100 to 200K	L	L	L
RS-422	N	M	100 to 1M	L	L	L
RS-485	Y	M	100 to 1M	L	M	L
CAN	Y	H	40K to 1M	M	M	L
USB	Y	H	900K to 480M	H	H	M
IEEE-1394	Y	H	100M to 800M	H	H	M
H = High, M = Medium, L = Low, Y = Yes, N = No						

Table 1: Serial Communications Features

The number of data words would also vary depending on the specific information being transferred. The data would be sent at a rate as determined by the AVC requirements.

Current serial interfaces being used in controller designs include RS-232, RS-422, RS-485, CAN bus, USB and IEEE-1394 (Firewire). Each of these interfaces has their own set of advantages and disadvantages. Table 1 summarizes some of the features of each of the interfaces.

E^3 (Electromagnetic Environmental Effects) The general definition of E^3 involves how a controller or system both affects and is effected by its electromagnetic environment. The electromagnetic environment involves both radiated and conducted fields. These fields can be either electric fields or magnetic fields. In addition, it is common practice to include the areas of lightning and/or Electro-Magnetic Pulse (EMP) and Electro-Static Discharge (ESD) as well. Each area needs to be considered by the designer during the controller design process.

For all military and commercial application, E^3 standards exist that must be met before the controller and/or system is qualified for use on the aircraft. Most US commercial aircraft follow the DO-160 standard. US military aircraft follow the MIL-STD-461 standard. In the case of US ARMY aircraft, an additional tailoring of the MIL-STD-461 to ADS-37A-PRF is applied. The UK standard applied to E^3 is the DEF-STAN-59-41. Each of these standards provides test levels of the allowed E^3 emissions from the actuation system. The standards also provide E^3 emission test levels that the actuation system must not be susceptible to. Table 2 below shows a summary of the various testing categories for each of the standards.

Test Type	DO-160D	MIL-STD-461C	MIL-STD-461D/E	DEF-STD-59-41
Conducted Emissions	Section 21.3	CE01, CE03, CE07	CE101, CE102	DCE01, DCE02, DCE03
Radiated Emissions - Electric Field	Section 21.4	RE01	RE101	DRE01
Radiated Emissions - Magnetic Field	Section 15	RE02	RE102	DRE02
Conducted Susceptibility - Power	Sections 17, 18, 20.4	CS01, CS02, CS06	CS101, CS114	DCS01, DCS02, DCS03
Conducted Susceptibility - Lightning / EMP	Section 22	RS06, CS10, CS11	CS115, CS116	DCS04, DCS08, DCS09
Radiated Susceptibility - Magnetic Field	-	RS01	RS101	DRS01
Radiated Susceptibility - Electric Field	Sections 19, 20.5	RS02, RS03	RS103	DRS02
Electro-Static Discharge	-	-	-	DCS10

Table 2: E^3 Requirement Standards

FGC Size and Weight Ask any aircraft manufacturer what is most important in a system design and the answer is guaranteed to be size and weight of the system. There are many systems vying for aircraft space and the smaller your system, the easier it is for the aircraft manufacturer to find a spot for your system. In addition, every aircraft would welcome the chance to save weight. Every pound saved is either another pound of payload or pound of fuel.

Major contributors to FGC size and weight are discussed in the following. This discussion is intended to portray trends and must not be used to specify an FGC size and weight. These design elements are interdependent and are also affected by other parameters such as vibration, shock and altitude requirements.

The controller designer must take the following into account during the design process. There are several factors that influence the overall size and weight of the controller. These factors include:

- The number of motor drive channels.
- The power required for each of the channels (Force Output).
- Thermal operating environment.
- E^3 requirements.

If the number of motor drive channels increases, the number of components increases, the input power requirement increases and the thermal loads increase. This will cause a necessary increase in controller size and weight (see Figure 12).

If the motor driver power requirement increases, the size and weight of the power devices will increase, the input power requirements will increase and the thermal loads will increase. This will cause a necessary increase in controller size and weight (see Figure 13).

If the thermal operating environment increases, additional or larger heat sinks may be required and power devices may need to become larger to meet thermal de-ratings. This will cause a necessary increase in controller size and weight (see Figure 14).

If the E^3 requirements are increased, this will necessitate the use of additional or larger input power filters and I/O signal filters. Again, this will cause a necessary increase in controller size and weight (see Figure 15).

All of these factors will influence the size and weight of the controller. As the requirement levels increase, the weight and size of the controller will also increase.

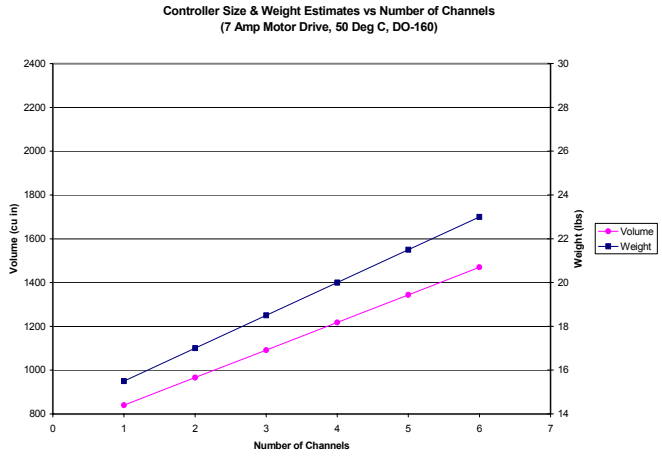

Figure 12: Controller Size & Weight vs Number of Channels

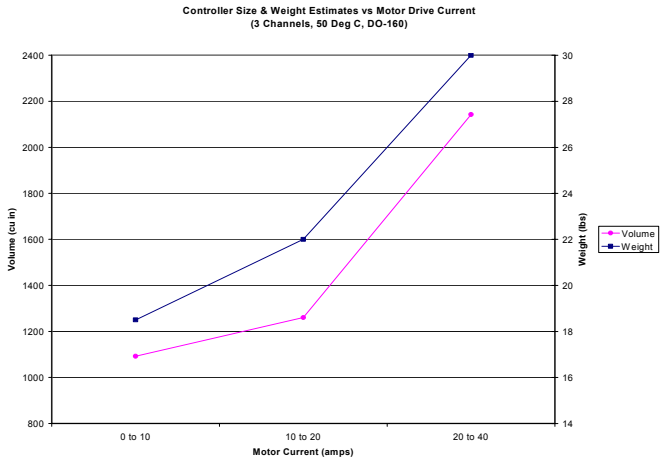

Figure 13: Controller Size & Weight vs Motor Driver Current

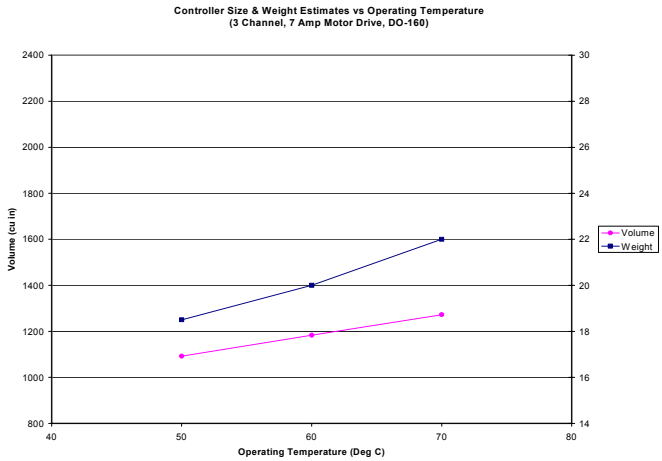

Figure 14: Controller Size & Weight vs Operating Temperature

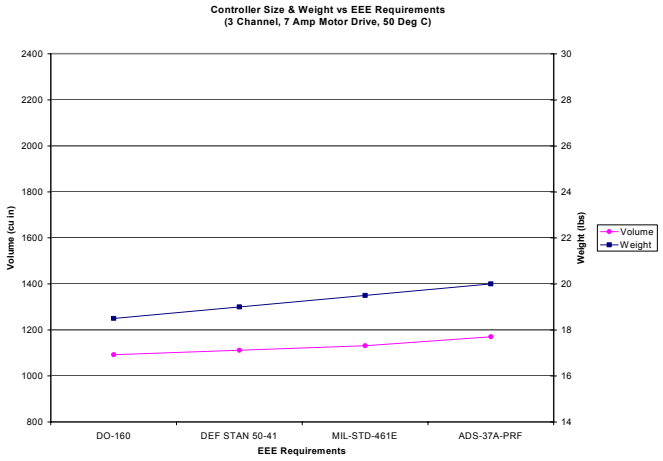

Figure 15: Controller Size & Weight vs E^3 Requirements

Current CRFG Applications

Moog's current CRFG systems include 1, 2 and 3 channels of FGs applied to several production helicopters. These systems have been qualified to typical helicopter environments.

Existing CRFG systems use various models of CRFGs capable of producing between 400 to 1700 pounds of force per FG. CRFG operating frequencies range from 14 to 24 Hz. Expanding the operating frequency is practical and under consideration.

In addition to applying the current CRFG systems to future aircraft a 6 channel system is being considered for development. This system will take advantage of the latest developments in DSP technology and power electronics.