- TRANSMISSION VIBRATION MONITORING - A SINGLE BOARD COMPUTER ARCHITECTURE

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ABSTRACT

In this paper, we describe the architecture of a digital signal processor module capable to perform the acquisition and conversion of vibration signals, coming from EH 101 helicopter transmission, to check and process the incoming data to obtain shaft "signature" parameters (unbalance, localize defects,...)
We include an analysis of the method used to obtain a sampling signal synchronous with the rotational period of each shaft.

1. Transmission Vibration Monitoring Requirements

One of the tasks required to the AMS (Aircraft Management System) of EH101 helicopter, as part of the Transmission Health Monitoring Package, is the Vibration Monitoring.

Vibration monitoring enhances the more traditional techniques; in particular this method make it possible:

- to detect some failures undetectables

- an early detection of failures or degradations

- a significant enhancement in terms of quality of assembly and manufacturing and availability of maintenance data during the operative service.

However the benefits described above will be obtained after an EH 101 maturity program, because the access, implementation and verification of the technical hypothesis is actually in development.

1.1 Method Description

The methods can be described as:

-the acquisition and conditioning of 13 accelerometers located in the Transmission System (Fig. 1) and 2 Azimuth Signals giving the time correlation with the main and tail rotors

-a processor unit to process converted accelerometers data according to the fault detection techniques; the processor type is selected having in mind the possibility to perform the analysis On Ground and minimizing the time required for On Flight analysis.

2. System Implementation

The above described functions will be hosted in the AMS allocating parts of its growth capability (Software and Hardware), minimizing the impacts on the actual system design.

The AMS is composed by

-two AMC (Aircraft Management Computer) and Control Panel

-two SIU's (Sensor Interface Unit)

The AMC performs all the major processing required for the air vehicle operation, such as helicopter system monitoring,

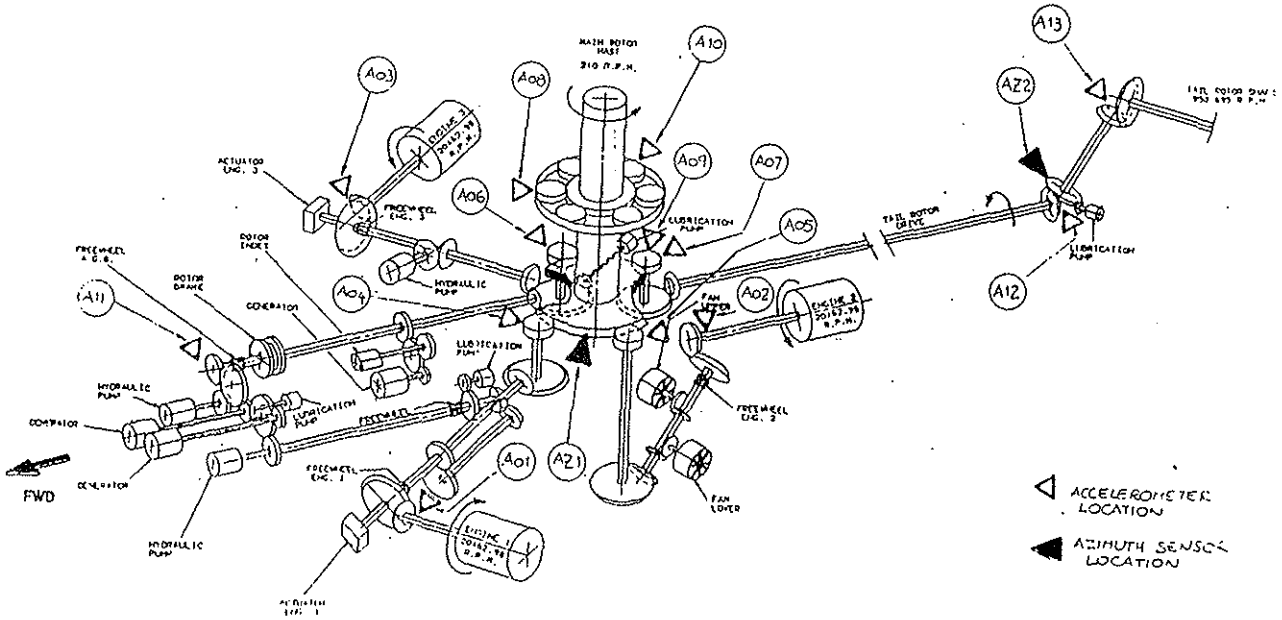

Figure 1: Transmission Assy.

advisory, caution and warning management, maintenance data recording, performance computations, pilot and copilot interface, etc. They also contribute to carry out the NAVS functions and manage the COMM subsystem.

The SIU interfaces and handles all the analog and discrete signals coming from the helicopter power plant sensors (engine, gearbox,etc.) and from the aircraft monitoring sensors; it serves as an interface for the AMC via a dual redundant 1553 bus.

The AMS diagram is shown in Fig 2.

Starting from this system organization and taking into account the great number of data to be processed, the implementation that minimizes the system overhead is :

-a self-contained hardware and software dedicated to the function adding a microprocessor based extra-board into the SIU

- a very simple protocol to interchange data and controls between SIU and AMC

- final task management (threshold and related caution) that, according to the normal functions, will be an application software program into the AMC

3. Module Performance and Interfaces

As shown in the introduction the core unit to implement the Transmission Vibration Monitoring, is embedded into a single board located inside the SIU.

This module interfaces:

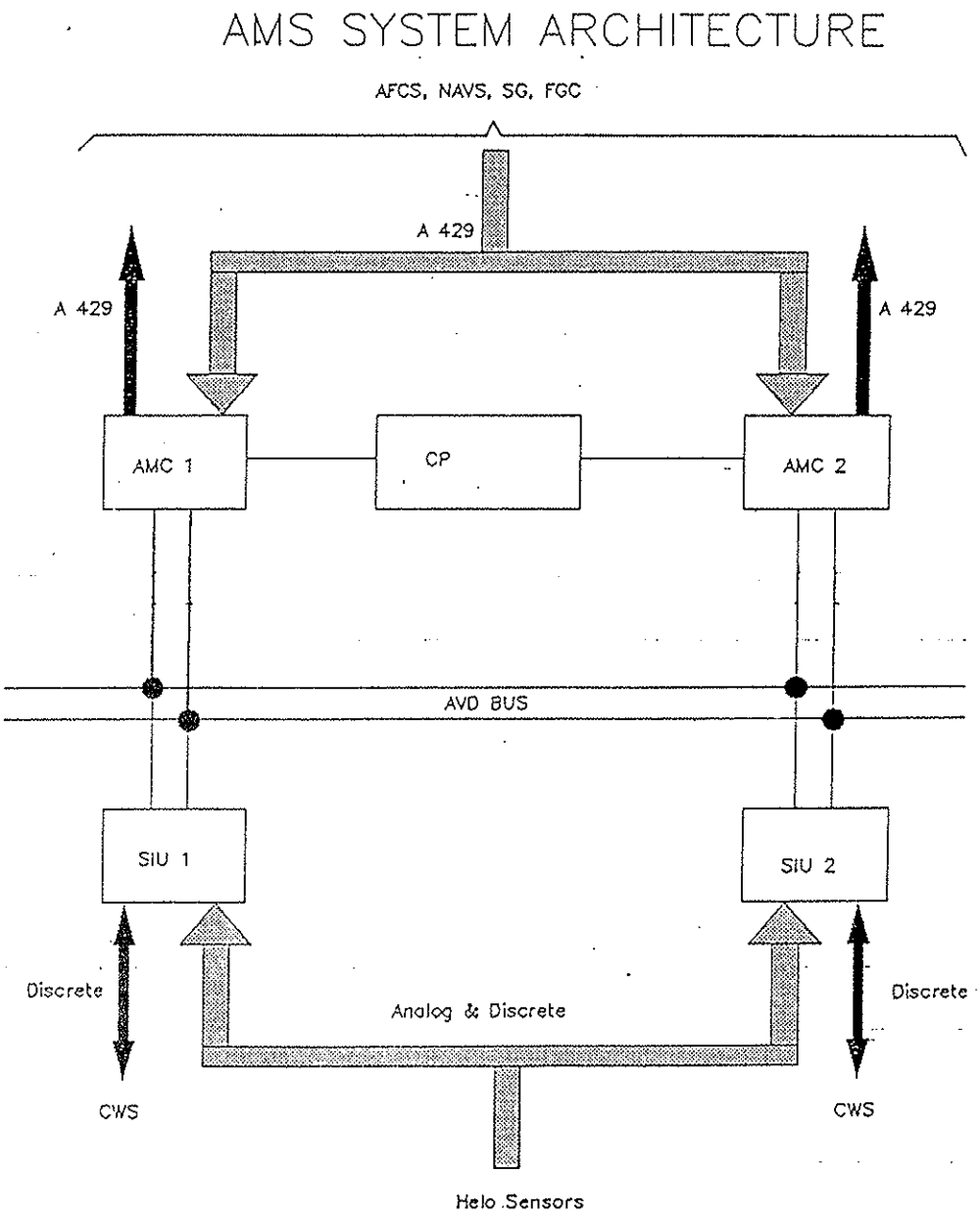

Figure 2: AMS

- 2 Azimuth Sensors

- 13 Accelerometers

- the SIU processor bus

and includes all the hardware facilities to allows the embedded software to perform the requested analysis (one analysis at a time).

Software task includes the application of Direct and Inverse Fast Fourier Transform methods; this approach means that the numbers of sample required for each shaft revolution are 2**N with N from 8 to 12 (up to 4096 points). So the frequency requested to sample the accelerometer is related to the shaft mechanical factors and, using as a reference the azimuth signals related to the frequencies of the main or tail rotor, is obtained using a PLL method as explained in the dedicated paragraph.
The PLL performances are also related to the software data preprocessing task: the

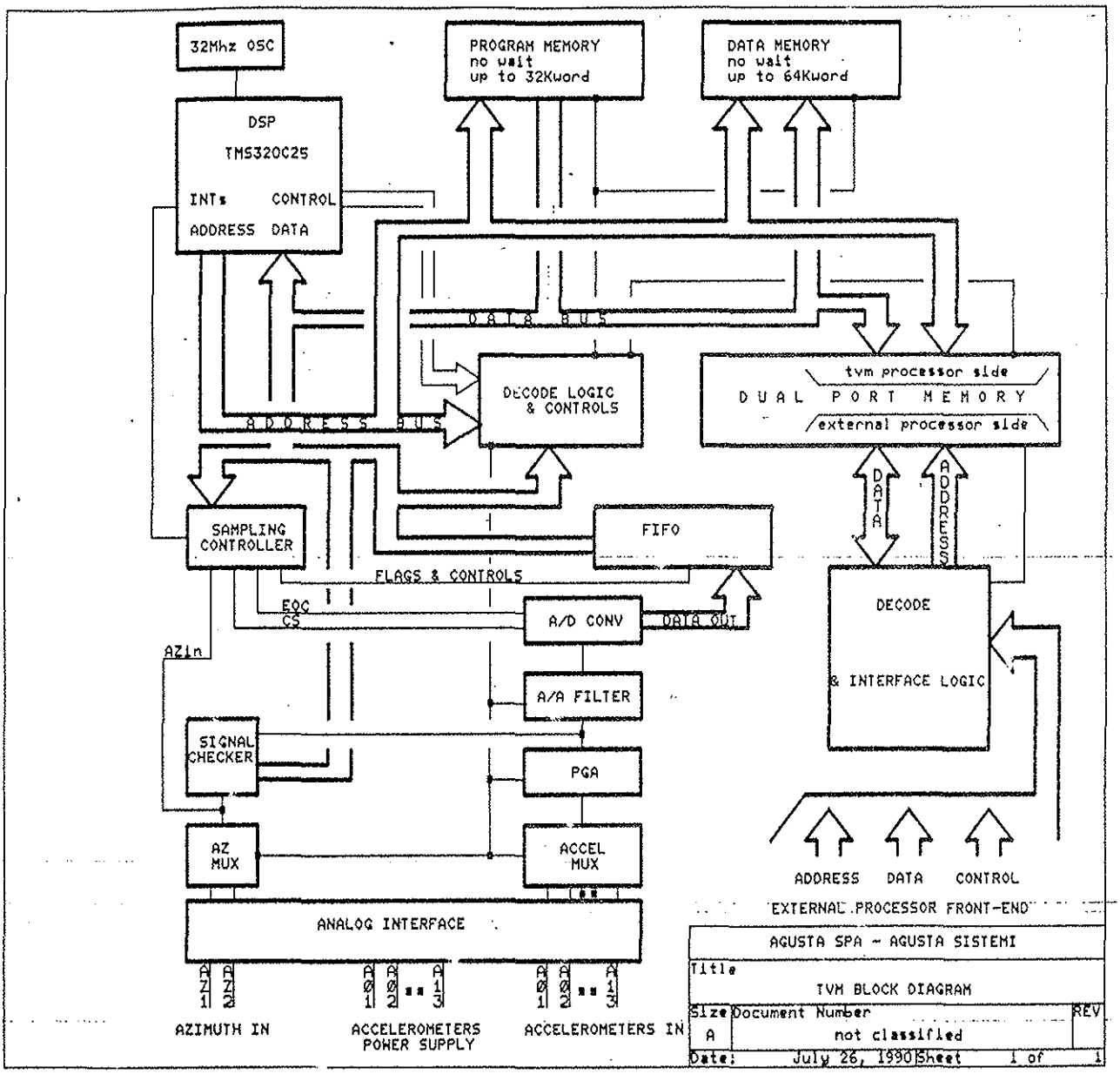

Figure 3: TVM Module

synchronous time averaging. The purpose of this process is to remove from a vibration signal the random noise and the periodic components not synchronous with the prescribed synchronizing period. This process is applied to each contiguous series (of 2**N points) to obtain the final averaged series. The averaging process is stopped when the current average is "very close" to the previous one.

The total processing to be performed (on-flight) can be split into the following main hardware and/or software sub-functions:

- conditioning and anti-aliasing filtering of accelerometers inputs
- sampling frequency generation
- analog to digital conversion
- synchronous time averaging
- signal demodulation
- parameter computation

- results loading

Conducting the above processing for all the accelerometers and different sampling frequencies (up to 44 analysis to be performed), the total time required is in the order of few minutes (this time is strongly dependent from the time to be spent to obtain the data convergence).

4. Module Architecture

The module architecture is shown in Fig. 3; it is composed of three parts:

- accelerometers and azimuth sensors interface; including sampling frequency generation and analog to digital conversion

- micro-processor block

- interface to SIU processor bus

4.1 Accelerometers front-end and filters

The accelerometers front-end module is a multiplexer used to select the requested channel and is connected to the processor programmable filter stage.

The front-end includes the necessary conditioning and de-coupling circuitry to interface the selected accelerometer. The selected output signal is connected, before filter, to a programmable gain amplifier (PGA) used during acquisition of low response accelerometer.

The anti-aliasing filters are seven four order Chebyshev type with cut-off frequencies comprised between 2.6 KHz and 31 KHz having ripple of about 0.1 dB. An integrated solution (i.e. a programmable switched capacitor filter) is actually in evaluation.

4.2 Analog to Digital Conversion and FIFO

This stage converts incoming analog data into digital data using one monolithic 12 bits ADC consisting of:

- ADC

- sample and hold amplifier

- microprocessor compatible bus interface

- voltage reference and clock generation circuitry

Main characteristics are:

- max. conversion rate: 200 KHz

- max. input range: +/- 5 volts

- twos complement data format (bipolar mode)

The ADC data bus is connected to a FIFO memory block of 2 x 4096 words; the FIFOs control signals are generated by a microprogrammed state machine that works synchronous with the end of conversion (EOC) signal ad allow a sequential FIFOs loading. The state machine handles the FIFOs addressing and generate interrupt to the microprocessor when the Full/Empty condition appears. Data are transferred into the data ram for processing; this method gives the best figure in terms of processing overhead during data acquisition phase.

4.3 Azimuth checker and Sampling Controller

This block contains the Azimuth Sensors front-end and selector, an ASIC (Application Specific Integrated Circuit), a dual VCO (Voltage Controlled Oscillator) and the necessary circuitry to perform the loop filters functions.

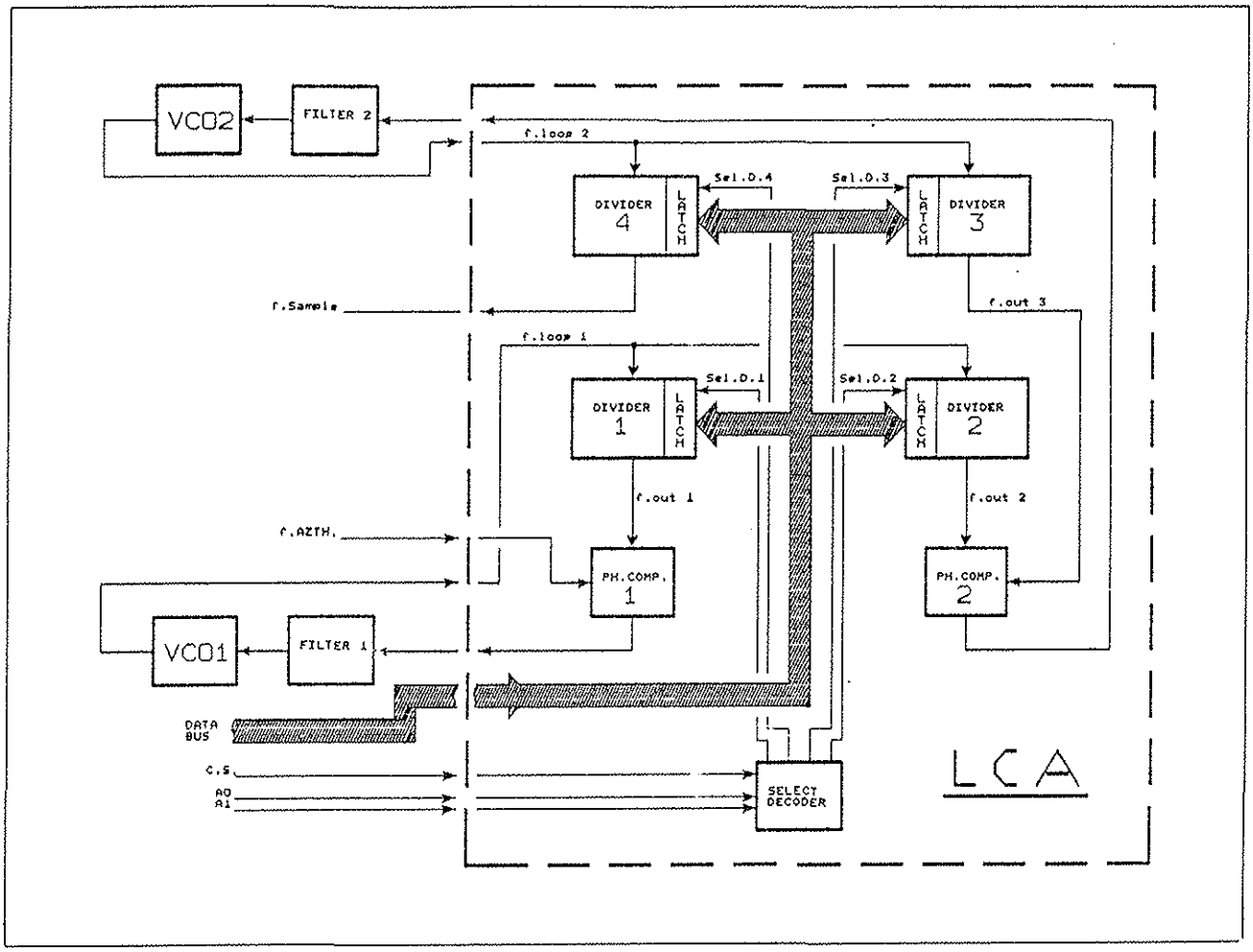

Figure 4: DPLL

The azimuth checker transforms, after filtering, the incoming azimuth signal (magnetic pick-up) into a digital pulse to be used by the sampling controller; the two azimuth nominal frequencies (100%) are: 2048 Hz for the main rotor and 1766.25 Hz for the tail rotor.

Starting from the azimuth signal the sampling controller generates the accelerometer sampling frequency as explained below:

the shaft frequency Fsh is provided by :

Fsh = Faz * NM / ND

with Faz = Azimuth Frequency and NM and ND are two integer numbers with no common factors.

The accelerometer must be sampled by a frequency NPT time Fsh where NPT = 2**N (NPT = 256...4096); then

Fs = NPT*Fsh = NPT*Faz*NM/ND

and Fs is the requested sampling frequency.

The Faz stability during the same analysis is in the order of 1%. The selected approach to generate Fs in all conditions is the use of two programmable digital phase-locked loops (DPLL).

The DPLL includes:

- two analog Voltage Controlled Oscillators
- two Loop filters
- the Logic Cell Array (LCA)

Inside the LCA, two phase comparators and four high-speed programmable dividers makes up the two loops as shown in Fig. 4.

The two phase comparators works in "phase and frequency" that means no phase error in lock condition. The phase comparator output consists in two signals that provide lead or lag indication of the input signal in comparison with the loop signal coming from the dividers.
The input signals are Faz for the first loop and Fsh for the second one.
The lead and lag flags are used to activate two three-state drivers that provides an high level signal
for the lag flag and a low level for the lead flag.
The operation of the phase comparator can be summarized as follows:

	Up Driver	Dn Driver
Lead	3-state	low
Lag	high	3-state
Lock	3-state	3-state

Wired together, these two lines are used to drive the loop filter.

The capacitor voltage of the low-pass filter is adjusted until the input and the loop signals are equal in phase and frequency; in this condition the drivers are off and thus the phase comparator output becomes on open circuit and holds the voltage in the capacitor of the low-pass filter constant.

In order to generate all the sample frequencies, the prescaling technique is used. The four dividers are set according to the NM, ND and NPT factors and the VCOs center frequency. All the dividers are loaded directly from the processor during the analysis initialization.

Like a microprocessor, the Logic Cell Array is a programmable driven logic device. The internal LCA design is controlled by a configuration program stored in an on-chip memory. The configuration program is loaded automatically from an external memory on power up or on command, or it is programmed by a microprocessor as a part of the system initialization.

The XILINX user-programmable gate array was selected after an evaluation of several types of programmable logic.

4.4 Processor

This function is the "core" of the module;it is composed by:

- DSP-CPU
- memories
- decode logic & controls

The block is based on the TEXAS TMS 320C25 16 bits DSP microprocessor CPU to constitute a computing system especially dedicated to mathematical processing as in this application.

This microprocessor offers the following main capability:

- Direct Addressing Capability: up to 64 Kwords Programs and 64 Kwords Data

- 32/40 MHz input clock

- 125/100 nsecs instruction time cycle

- computing capability up to 8/10 Mips

- 32 bits ALU and accumulator

- bit-reversed indexed addressing mode for radix-2 FFT

- on chip timer for control operation

- 3 external user maskable interrupts

- serial port for direct communication (up to 5 MHz bit clock)

- instruction set (up to 133 instructions)

The microprocessor dedicated memories are:

- 32 Kwords (2 x 32 Kbytes) EPROM program memory (no wait state) with access time of 45 nsecs.

- 64 Kwords RAM (4 x 32 Kbytes) memory (no wait state) with access time of 45 nsecs.

to allow the maximum use of the microprocessor potentiality.

4.5 Bus Interfaces

The nodal bus interface block is composed by:

- a Dual Port Memory (DPM)

- Decode and Interface Logic

to allows the data exchange and the mode setting between the SIU processor (connected to the AMC via 1553 bus) and the TVM module. The decode and interface logic controls the correct addressing of the TVM module and it is compatible with a single or a multi micro processor structure. The DPM memory size is 4096 words.

4.6 BITE Philosophy

An extensive BIT will be inserted to permit failures detection at module level using the microprocessor facilities and dedicated BIT routines.

BITE philosophy includes:

- electrical and frequency check of azimuth

- accelerometers peak voltage check

- PGA gain test and ADC linearity

- LCA program test

- VCO test

in addition to the normal microprocessor test like:

- instruction set test

- program memory check-sum

- ram test

- decode logic test

5. Software Structure

The software residing inside the TVM Module has been divided into different functional groups: Interrupt Routines, I/O Handlers, Services Routines, Application S/W as depict in Fig 5. The selected program languages are Assembler and C.

The two interrupt routines are: Power-On and FIFOs management.

POWER-ON is a routine connected to the Master Clear signal generated by power supply control module; the main tasks are :

- software initialization
- hardware initialization
- LCA program loading
- off-line BIT

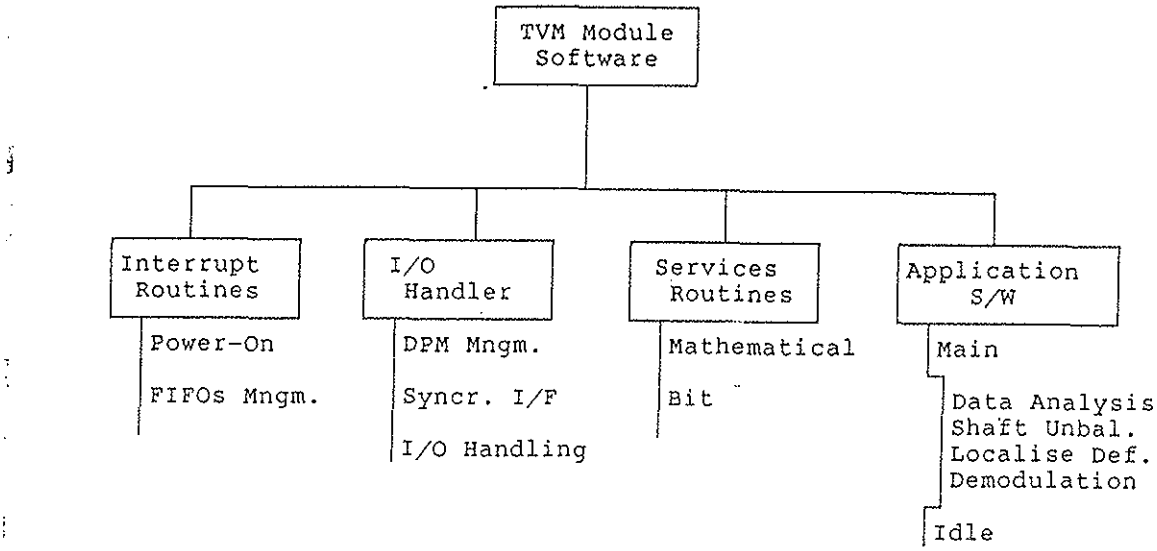

Figure 5: S/W Break Down

FIFOs Management is charged to handles the data transfer from the FIFOs and the microprocessor data ram.

The I/O handler functional group includes the drivers for the hardware interface modules

- Dual Port Memory handshaking control

- Synchronization I/F for PLL and Azimuth

- I/O handling dedicated to the module front-end configuration

The service routines group includes the sub-routines common to different programs like mathematical routines and BIT.

In particular:

FFT
FFT-1
arctang
RMS
P-P
SQRT
etc..

The main program is structured following the algorithm requirements.

- Data Analysis
- Row Data Diagnostics
- Synchronous Time Average
- FFT
- Shaft Unbalance Fault Detection Technique(FDT)
- Localized Defect Enhancement FDT
- Demodulation FDT

5. Conclusions and future trends

This architecture offers the possibility to implement in a single avionic standard module all the main processing functions required for the EH 101 Transmission Vibration Monitoring. However this architectural structure having powerful capabilities in terms of processing and modularity and offering embedded hardware reconfigurability provisions, could be easily modified to accept other helicopter functions (i.e. rotor tracking and balance). Future trends are mainly related to a more powerful processor supporting ADA factory.