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.

OPST 1

A DIGITAL OPTICAL TAIL ROTOR CONTROL SYSTEM

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<u>ABSTRACT</u>

OPST 1, a German acronym for Optical Control System, Phase 1, is the working name for a technology programme of the German Ministry of Defense. In this programme, MBB and the DFVLR are investigating the application of optical signalling and new micro-electronics for future helicopter controls. Presently the main work package is the development and flight testing of a production-oriented digital redundant "fly-by-light" tail rotor control with full authority. Simultaneously, an experimental 4-axis fly-by-wire/-light flight control computer for future research is being developed and will be tested, alternatively to the dedicated yaw control computer, in the tail rotor mode. The programme is conducted in co-operation between the DFVLR and MBB with Liebherr-Aero-Technik (LAT) as subcontractor.

This paper gives a summary of the present status which is characterized by the availability of new qualified hardware and software, and imminent flight tests on a BO 105 demonstrator. It describes the general programme and design goals, explains the more important technical solutions and concludes with prospects for the near future.

1. GENERAL CONSIDERATIONS

- The flight behaviour of the helicopter with one main rotor the most common type - is characterized by some properties which make helicopter flying a more demanding task than flying an airplane. Main problems are coupling effects and dynamic stability. In other words, a pilot's command in one control axis will normally induce a coupled motion in other axes. On the other hand, an external perturbation, say gust, will usually produce not only a motion in the direction of perturbation, but also a complex motion in all other axes.
- In simple missions without stability augmentation system, the pilot has to assume all the stabilizing functions. This is acquired by special training, which produces the required reflexes. For more demanding missions, in which the pilot has to take over other tasks than simple flying, it is state-of-the-art to use stability augmentation systems (SAS) in simplex, or even duplex redundant form, acting either on the tail or the main rotor or both. Depending on the degree of redundancy, the rotor control authority of such SAS is limited, for a tail rotor with duplex SAS to typically 40% of the tail rotor authority.
- These general considerations lead to the idea of putting some automatic devices between the pilot and the rotors, which are capable of taking over <u>all</u> the stabilizing and decoupling functions with a high overall safety, thus decreasing the pilot's workload dramatically. This implies control systems with full authority and redundancy. Modern electronics is able to deliver the necessary computing power.
- All these above-mentioned arguments are equally valid for fly-by-wire. With fly-by-wire, one of the most challenging threats is the electro-magnetic environment which has to be counteracted by means of shielding, bonding, filtering etc.. Here, optical data transmission offers a substantial relief. Furthermore, with optical data transmission, data rates of more than 10 times of those of wire can be utilized.

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2. DESIGN CHARACTERISTICS

- The yaw axis was chosen for OPST 1 because:
 - * only one actuation system must be installed
 - * only fail-operative fail-safe behaviour is required
 - * simple integration into the helicopter
 - * all critical aspects of optical data transfer can be investigated
 - * cost and risk are minimized
 - * control response decoupling and their effects on pilot's workload can be demonstrated
- The primary requirements for such an improved tail rotor control system are:
 - * Rate demand via pedal inputs in hover and sideslip in cruise
 - * Increase in yaw stability and yaw accuracy
 - * Insensitivity to lateral gusts
 - * Quasi-automatic yaw trim
- As a consequence of the above requirements, the tail rotor control system must offer more than 40% authority, since there are several manoeuvres requiring higher degrees of authority for stabilization and decoupling. This in turn requires at least a triplex design for electronics, position sensors and motion sensors. With such a triplex full-authority electronics, a fail-operative fail-safe characteristic is achieved. In order to provide the same characteristic for the actuator, duplex hydraulic supply and duplex actuator are required. This fail-operative, fail-safe behaviour of the triplex design, paired with the self-centering properties of the tail rotor, permits standard emergency procedures not very different from the procedure after loss of the tail rotor drive. In this context, it is worth pointing out that helicopters, in contrast to airplanes, never have control surface redundancy: rotors are simplex.
- A further design aspect is the communication between the components of the control system. The flight control computer, the sensors and actuators have to exchange digital messages. The classical way is electrical signalling as it has already been realized in fighter and transport aircraft. Despite the fact that fly-by-wire has reached production maturity, there still remains the burden of a good electro-magnetic compatibility (EMC) design providing not only shielding, bonding and filtering, but also ensuring its full functional capability during the total life of the aircraft. All components required for the electro-magnetic interference (EMI) suppression must be separately tested, otherwise any loss of protection will only be detected when the system is exposed to EMI with the possibility of immediate failure. Optical data transmission is inherently immune against EMI. However, additional experience is required especially with respect to production handling of the fibres and connectors. Only when these data become available from this programme, a final comparison with respect to weight, volume, power consumtion, reliability, cost and cost of ownership etc. can be made. That's the reasons why we decided to use optical signalling.
- MBB is therefore aiming at a production-oriented tail rotor control design, whilst the emphasis of the DFVLR activities within the programme is put on the aspects of a fault-tolerant 4-axis flight control system for research application.

3. SYSTEM ARCHITECTURE, YAW AXIS CONTROL SYSTEM

- OPST 1 has the usual control loop consisting of pilot's input transducers, control and display unit, flight control computer (FCC), actuator and yaw rate gyros (fig.1). With his pedal inputs the pilot commands practically a yaw rate in hovering and low speed flight, which necessitates some data processing in the FCCs in order to provide good handling qualities. In the case that there is no pedal input, the FCCs will command the actuator such as to keep the yaw deviation, given by the yaw-rate gyros in reference to the old yaw position, to zero.



- The hardware is of triplex design for the FCCs, the position pick-offs and rate gyros, and duplex design for the hydraulics, with duo-duplex electronics for loop closure and monitoring. Each channel is independent of the others. The only cross-channel communication takes place between the three FCC channels (or lanes). The input and output signals in the FCCs are consolidated by voter functions as well as the input signals into every actuator half. There is no cross-communication between both actuator halves.
- The data transfer is made by means of fibre optics. Since there is no need for a global signal distribution, we adopted a point-to-point signalling, avoiding the use of a complex optical bus. A block schematic of the signal-flow structure is given in fig. 2. It is worth pointing out that the cross-channel communication between the FCC lanes is also realized by means of optical fibres, thus providing total electrical isolation between the channels.



- As shown on fig. 1, OPST 1 is to be flight tested with a mechanical back-up. This mechanical back-up, however, is only available to the safety pilot. Using safety controls is an effective approach for flight tests on a demonstrator. It contributes to saving development cost and time, avoiding an extensive certification work, and provides a possibility for system verification in flight.
- The DFVLR has designed a fault-tolerant 4-axis multi-processor system named DISCUS and built up a ground based simulation facility. LAT is responsible for the actuator with integrated electronics and for the DISCUS development. MBB's share includes development and manufacturing of all other parts of the system, yaw axis system integration, aircraft modification and the overall system responsibility. DISCUS and the dedicated yaw control computer are fully interchangeable in the tail rotor mode.

4. HARDWARE OF THE YAW AXIS CONTROL SYSTEM

- This section describes the main hardware elements of the yaw axis control system.
- Yaw Control Computer (figs. 3.2, 4)
 - * The MBB production-oriented FCC is a derivative of the computer developed for the EMI Fault Protection and Self-Recovery Digital Flight Control System presented at the 12th European Rotorcraft Forum (ref. 3). It makes use of the M 68000/68881 micro-processor running at 12.5 MHz. Its 8 kByte real-time programme is executed within 3 ms. This permits not only the execution of various control laws, voting and monitoring functions and failure management, but also to perform extensive digital filtering for structural mode suppression.
 - * The data are exchanged between the 3 lanes via a 1Mbit/s serial optical link with a Mil-STD-1553 B protocol. Signal transfer from and to the other components of the flight control system is by means of 28 bit/optical serial data

links at 1Mbit/s with a special dedicated protocol.

* All optical modules are of standard MBB design and build. The FCC is programmed in the structured high-order language C with some special functions in assembler.

- Rate gyros (fig. 3.6)

- * Each unit contains 3 identical-oriented rate gyros of conventional technology since optical rate gyros are not available on the market. No effort was undertaken to build special optical pick-offs, but the signals are converted within the gyro package into optical information, using the standard MBB optical modules described below.
- * Full mechanical and electrical isolation between the 3 lanes is provided for.
- Position sensors (figs. 3.4, 3.5)
 - * 3 parallel linear variable differential transducers (LVDT) with their assiociated electronics are mounted within one housing. Again, the electrical signals are converted into optical ones by the optical modules. Full mechanical and electrical isolation is provided for.
- Actuator (fig. 3.3)
 - * The LAT built and designed actuator is derived from an earlier experimental programme. Since the technical problems assiociated with such duplex tandem hydraulic actuators are state-of-the-art and their design very specific to the application, no special effort was undertaken to optimize its mechanical design. The real novelty is that it has been modified to a "Smart Actuator".
 - * All the interface electronics including servo loop are integrated into the actuator housing. Each half of the actuator is controlled, voted, monitored and tested by 2 micro-processors M 68000 in a real-time cycle of less than 2.5 ms.
 - * Each lane of the FCC is optically connected to each actuator half via the MBB optical modules. A 4th optical modul per side is used to transfer actuator status information back to each of the FCC lanes for degradation management.

- Optical signalling

- * The fiber selected is the high-purity multimode step index type with 200/280 µm cross-section. It was selected because of its high mechanical strength, robustness and chemical immunity, as well as its wide temperature range (-50C to +150C). Also experience gained from fighter aircraft experimental tests supported this decision. The connectors are of Mil-C-38999 Series IV standard.
- * The optical components from which the optical modules (fig. 5) are built were specially designed and qualified by MBB for this application. Being hermetically sealed, they have a wide temperature range from -55C to 100C, with the receivers extending up to 125C. With exterior dimensions of approx. 20x15x5 mm, they are easily accommodated directly on the printed-circuit boards (fig. 4). The data rate of 10 Mbit/s has been established at a wave length of 960 nm. Choice of wave length was made due to low power consumption and high stability. Production problems have been successfully solved and medium size batches are being produced of consistant quality. During direct lightning tests, no failure of the modules was observed apart from external housing burn marks.



Fig. 3: OPST 1, System Installation on Demonstrator



Fig. 4: OPST 1, Triplex Yaw Control Computer



Fig. 5: OPST 1, Miniaturized Optical Modules left: receiver, right: sender

5. <u>DISCUS: AN EXPERIMENTAL FAULT-TOLERANT 4-AXIS</u> <u>FLY-BY-WIRE/ FLY-BY-LIGHT CONTROL SYSTEM</u>

5.1 Objectives

- Within the joint programme, the DFVLR has designed the fault-tolerant 4-axis flight control system DISCUS for experimental use. The acronym DISCUS stands for "Digital Self-healing Control for Upgraded Safety". The main objectives of the DFLVR task are:
 - * Research and investigation of alternative methods to improve the integrity of flight control systems without increasing the redundancy level (methods of redundancy management e.g. analytical redundancy and pre- and in-flight monitoring)
 - * Development of advanced control laws to improve the handling qualities and thus to reduce the pilot's workload
 - * Investigation and testing of new hardware technologies and components for fly-by-wire/ fly-by-light flight control systems (sensors, data communication, multi- processing in flight-critical applications, actuators)
- The key element of the DISCUS project is the fault-tolerant flight control computer system. To carry through research tasks concerned with fault-tolerance and redundancy management, a certain redundancy level is required but there is no need to meet the safety requirements of a fully operational system. The computer is designed as a modular experimental system aimed at the above-mentioned objectives. The major design requirements were:
 - * One-fail-operational
 - * Low probability of total loss
 - * Modular hardware design with adaptability to future research projects. Compatibility to a commercial standard
 - * High computing power, multi-processing capability
 - * Intensive use of a high-order language; only low-level interface drivers written in assembly code
- With a triplex architecture of the FCC the one-fail operative capability is achieved by conventional methods of redundancy management (static redundancy). With additional in-flight computer self-tests and monitoring of the inputs and outputs, it might be possible to built a computer system with a single-channel fail-safe capability, which is one of the DISCUS objectives. Besides this, a further item of investigation is the redundancy management of a multiprocessor system and the feasibility of reconfiguration in case of the loss of one processor.

5.2 System Design and Architecture

- Substantial reasons for the selection of the DISCUS system architecture were the method of monitoring, the desired one-fail-operative capability, the possibility to perform the planned research tasks, hardware flexibility and modularity and the existing servo-actuators. Figures 1 and 2 show the general architecture which is common to the yaw control system and the 4-axis control system.
- DISCUS consists of three electrically isolated parallel channels or lanes (fig. 6).
 Each lane comprises 3 Single Board Computers (SBCs). Each SBC consists of a Motorola 68020 microprocessor with a 68881 math co-processor, local memory,

programmable timers and serial and discrete I/Os. There are two means of communication between all the SBCs in the redundant system:

- * Within one lane Intralane Communication a 128 k-byte Global Memory is provided to exchange and share data between the SBCs.
- * Between the three lanes, the data exchange is provided by a conveniently named Interlane Communications card.



Fig. 6: DISCUS, System Architecture

The Intralane data transfer between SBCs, Global Memory and all interfaces is accomplished by a 16-bit parallel VME-bus. All boards are plug-compatible to the commercial VME-bus Standard, but shorter in height to fit into ARINC boxes. Within each lane each SBC has equal rights to read data from or write data to the Global Memory.

The specifically designed Interlane Communications card drives the fibre optic links from each lane to the other two lanes. Transmission is of serial type following the ARINC 429 Standard. Data is broadcast from one lane to the others. Each Interlane card has a 1k-word mailbox memory for the in-coming data received from the other lanes.

- Since DISCUS is designed for different research applications, the computer provides a set of standard and nonstandard interface cards for optical, analogue, discrete, ARINC-429 and MIL-1553 inputs and outputs. For the yaw control application, the fibre-optical interfaces are used for data communication with sensors and actuators, while for 4-axis activities most of the other interfaces are required. DISCUS was designed by DFVLR and developed by LAT. Fig. 7 shows one lane of the flight control computer.



Fig. 7: One Lane of the DISCUS Computer Hardware

5.3 Software

- The Executive of the flight-operational programme, designed for a 4-axis system, is the top-level software which controls the entire system. In each lane of the triplex system, identical software is loaded. Maximum performance is achieved by separating the software tasks between the 3 SBCs and operating them in parallel at appropriate cycle rates.
- In the basic 1/1 control mode the pilot's command inputs are consolidated, transferred to the command output and, before being sent to the actuators, once again consolidated. Application-dependent flight-control software presently the yaw control laws is embedded into the basic mode and selected through the Control and Display Unit by the pilot. Fig. 8 shows the general data flow.



Fig. 8: Data Flow of the DISCUS System

- Synchronization

The three lanes of DISCUS are frame-synchronized to accomplish cross-channel monitoring of all inputs.Each SBC synchronizes with all SBCs in its own lane as well as with those in the other lanes. Thus a single fault in the synchronization of one SBC does not procure a total loss of one lane but just the loss of this specific SBC.

· Cross-Channel Monitoring (Voting/Monitoring Function)

For fault detection and isolation the three lanes have also to exchange their data via the Interlane Communications card to perform cross-channel comparison. In each lane the own data are compared with those received from Interlane. The monitoring of the data is accomplished by two different methods:

- * The first method is the cross-channel comparison with threshold values. This is used for all sensor signal inputs. The algorithm employed always selects the mid-value as the "true" one which should be identical in all three lanes.
- * The second one is a cross-channel comparison with bit-by-bit voting. This is applied to those data which have been derived from inputs consolidated by the first method before. The "true" value is selected by majority voting. This method is applied to the integrators and the output signals.

Applying these two methods for cross-channel comparison reduces the difficult task of defining thresholds to a limited number of inputs. It also simplifies the software function and increases computing efficiency. Bit-by-bit voting requires data of equal frame cycles to be compared.

- Fault Management

The results of all monitoring functions in the flight software are written into an Error Matrix in the Global Memory. Detected and acknowledged errors are indicated to the pilot by the Fault Indicator Lamps in the Control and Display Unit. Each lane has its own lamp in this Fault Indicator. An error is detected if one of these lamps is on.

- Start-up BIT and Pre-Flight Check

After "power-up" each SBC performs a Start-up Built-in Test (SUB), which is a lane self-check. An overall system test before take-off is the Pre-flight Check function (PFC). While the SUB is running asynchronously, the PFC requires a synchronized system. The tasks of these tests are separated between the SBCs within one lane. One goal of the SUB and PFC is to ensure system safety and the absence of dormant errors before take-off.

6. GROUND TESTING ENVIRONMENT

- To validate the flight software on ground, a testing environment has been built up. This comprises all the helicopter-system interfaces with the original redundancy level, a simplified non-linear helicopter simulation, a simulation of sensor and hardware errors, interfaces for general purpose test equipment, data links to a helicopter mock-up and an enhanced simulation facility. Moreover, original hardware as inceptors or actuators may be included in the ground tests.
- A schematic representation (excluding the data link to the enhanced simulation) of the ground-test environment is shown in fig. 9. The essential portions of the test equipment are:
 - * Helicopter Simulation Terminal Computer (HST)
 - * Test Control Panel
 - * Error Display Unit
 - * Quick-Look Recorder
 - * Control and Display Unit
 - * Pilot Controls Mock-up
 - * Actuator Test Rig
 - * Triplex Flight Control Computer



Fig. 9: Schematic Representation of the Ground-Test Environment

- Helicopter Simulation Terminal

The HST is a computer system which comprises all those sensor data with the required redundancy level which are necessary to perform ground testing of the 4-axis FCC. To meet the real-time requirements, a simplified non-linear simulation of the BO 105 test-helicopter dynamics is running for control law evaluation.

• Fault Simulation

To prove correct system behaviour in case of a fault, a simulation facility was integrated into the HST software to generate different kinds of faults. Presently, there are three types of faults which may be initiated by command input from the Test Control Panel:

- * Sensor faults
- * Control and Display Unit faults
- * Specific hardware faults in the redundant computer system

Specific hardware faults in the FCC may be controlled via the HST. This is accomplished by additional software implemented for test purposes only. Initiation of a fault is performed by a code sent from the HST to the FCC. This type of fault simulation is only applied to those hardware elements related to software modules which carry out the lane synchronization and the cross-channel monitoring.

- Error Display Unit

As mentioned above, the indication of a detected error in the redundant computer system is performed by switching on the Fault Indicator Lamps in the Control and Display Unit. Moreover, information about the type and location of the error is derived from an error analysis, run in each lane of the FCC. To demonstrate system reaction, a textual and graphical representation of the analysis on an Error Display Unit is installed.

7. STATUS OF TEST AND INTEGRATION

- MBB Yaw Axis Control System

- * The integration of the system in the laboratory has been successfully completed with the yaw control computer. This confirms that the first level software validation has been successfully achieved in both the FCC and actuator. Among other qualification tests, EMI tests have demonstrated the insensitivity of the yaw control system to hight electro-magnetic field strengths of more than 150 V/m in the high-frequency range (ironically, the only limitation encountered by now was caused by the test house).
- * Several problems with crimp connections of the optical cables were encountered, which will need further attention in follow-on programmes.
- * Even though not of particular relevance to this application, the optical signal attenuation experienced in the connectors will also need further investigations. New technologies like optical lenses in the plugs should reduce this problem drastically.
- * Also the first experiences have been gathered to respecting minimum bending radii. They have to be fed back to the design offices as well as fed forward to the production floor.

DFVLR DISCUS

Concerning DISCUS, the 4-axis 1/1 and the yaw axis control modes, including full redundancy management and error analysis, have been successfully tested on ground.

- Integration in BO 105-S3

The demonstrator, a BO 105 belonging to the DFVLR, is being modified at MBB for flight tests. The yaw axis control system is currently undergoing integration and acceptance tests.

- Flight tests

Initial functional tests will be performed at and by MBB. The helicopter will be then transfered to the DFVLR for further functional tests and flight trials.

8. PROGRAMME PROSPECTS

After more than 2.5 years of development, both hardware and software are now available for flight test evaluation of the yaw axis.

The triplex DISCUS system, after having been tested in the tail rotor mode, thereby partially verifiying the redundancy management and error analysis, will be used for further research applications at the DFVLR.

The expertise thereby gained by the 3 participating companies is now beeing applied to the definition, design, development and flight testing of a complete "fly-by-light" 4-axis quadruplex control system oriented at the "Helicopter 2000".

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